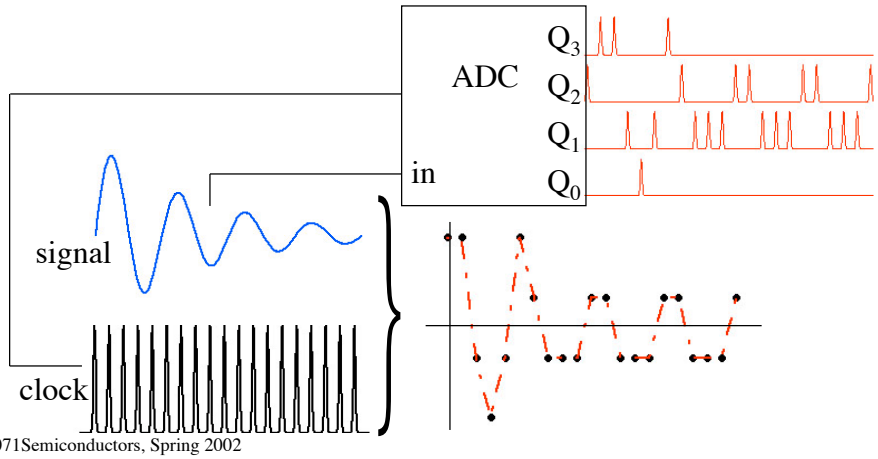
Analog to Digital Conversion

So far we have mostly discussed continuous (analog) signals, but today most computation and measurement is carried out with digital systems. So, we need some means of taking an analog signal and digitizing it.



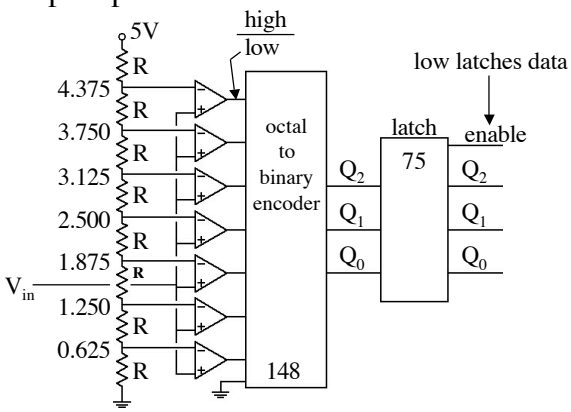
To digitize a signal we need a time base and an Analog to Digital Converter (ADC) that provides a digital approximation of the original signal. The digital approximation is recorded in N - bits (in this case 4) and the variation can be recorded to an accuracy of at best 1 part in 2^N. The time base determines how quickly we can sample the waveform and varies greater with type of ADC. It is possible to have 24 bit accuracy and frequencies of 1 GHz, but not simultaneously. In general the greater the number of bits, the slower the device.

The most significant bit (msb) is the one recording the highest voltage variation and the least significant bit (lsb) records the smallest voltage variation.

Analog to Digital Conversion (cont.)

The simplest A/D conversion to understand is perhaps the flash conversion.

This uses a set of analog comparators very similar to what we saw in the op amp lecture.



The flash digitizer is only very rarely used but it is the simplest to understand. It is just an array of comparators and the output simply tells in which voltage range the input appeared. The trick is to have a set of precise resistors so that there is a well defined ladder of voltages. The output of the comparators needs to be converted to a binary number and then stored temporarily until it is read into a computer etc. The change in coding will be covered in latter lectures.

Flash Converter Table

V_{in}	OA_7	OA_6	OA_5	OA_4	OA_3	OA_2	OA_1	OA_0
<.625	0	0	0	0	0	0	0	0
1.250	0	0	0	0	0	0	1	0
1.875	0	0	0	0	0	1	1	0
2.500	0	0	0	0	1	1	1	0
3.125	0	0	0	1	1	1	1	0
3.750	0	0	1	1	1	1	1	0
4.375	0	1	1	1	1	1	1	0
>4.375	1	1	1	1	1	1	1	0

This just shows in more detail the outputs as a function of the input voltage. Note the only information is “what is the most significant bit that is set?”

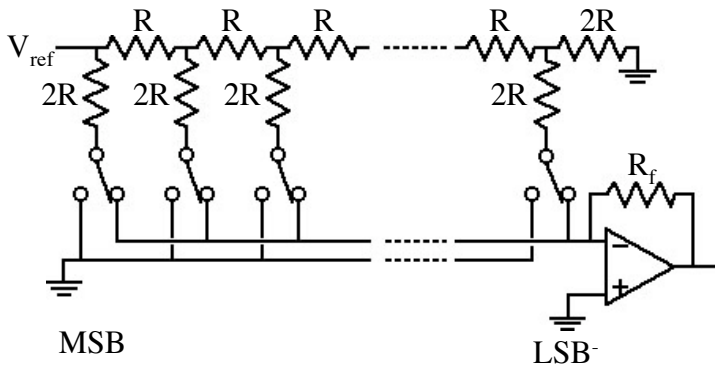
Flash Converter (cont.)

- benefit of high speed
- however many comparators
  - 8-bit requires 255 op amps on a chip
  - large power dissipation
- Example:
  - Datel ADC-208
    - 8-bit @ only 50ns
    - or 20,000,000 samples per second
- More often flash converters are used with a sample & hold, and scaling
  - Analog Devices AD733A
    - 10-bit @ 50ns
    - with only 48 op amps.

If you really want to go fast and heat and cost are not issue this is the device for you.

D/A Converter

Most A/D converters include a D/A converter and a comparator.



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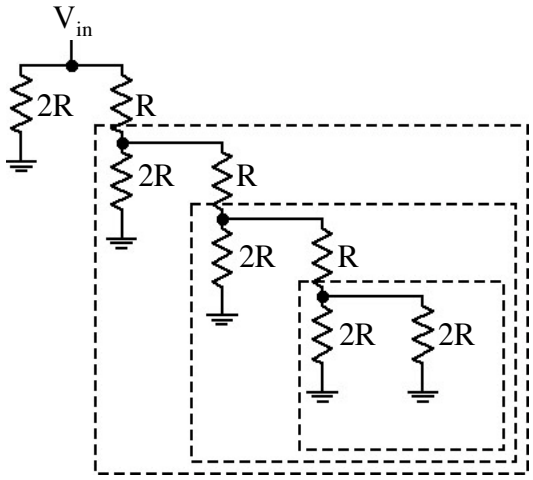
To understand how most useful ADC work, we first need to look at the opposite problem of how do we take a digital word and convert this into an analog signal. This can easily be accomplished in a single step, again using a ladder network of resistors. Here the ladder network is to create a voltage divider. Recall that the importance of a signal going into an op amp depends on its source impedance (the current in is what matters). Here by setting the switches we choose how important each stage is.

The switches are of course controlled by the logic and are most conveniently some type of FET.

D/A Converter (cont.)



2R || 2R ⇒ R
R Series R ⇒ 2R

The current splits into two paths at each node. Recall, the output of The op amp is proportional to the current.

This ladder network has the nice property of always looking like a by 2 divider. Since we are using a binary coding, by 2 is convenient.

D/A Converter (cont.)

The total current flowing into the op amp is

$$I_{total} = \left[S_N \cdot 1 + S_{N-1} \cdot \frac{1}{2} + S_{N-2} \cdot \frac{1}{4} + \cdots + S_1 \cdot \frac{1}{2^N} \right] \frac{V_{ref}}{2R}$$

$S_1 \equiv$ switch for least significant bit.
$S_N \equiv$ switch for least most bit.

Let's rescale this by $\frac{2^{N-1}}{2^{N-1}}$

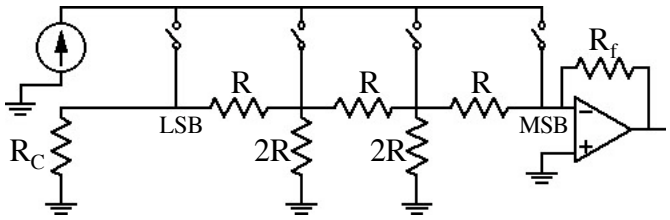
$$I_{total} = \left[S_N \cdot 2^{N-1} + S_{N-1} \cdot 2^{N-2} + S_{N-2} \cdot 2^{N-3} + \cdots + S_1 \cdot 1 \right] \frac{V_{ref}}{2^N R}$$

We recognize that $S_N \ldots S_1$ simply correspond to the binary representation of V_{ref}.

Given a ladder of divide by two networks a binary coding of information is the obvious choose.

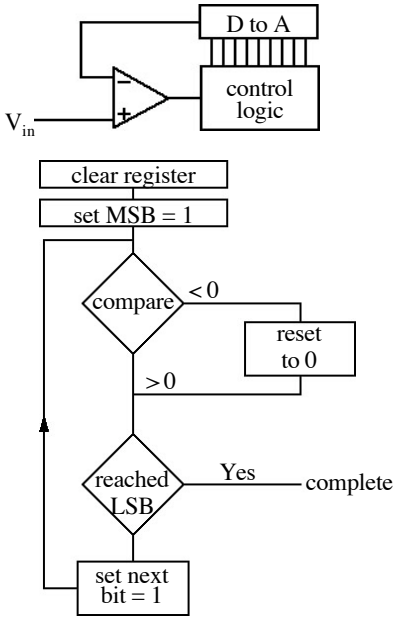
Problem

Show that if you wish to measure a current rather than a voltage



Here you need to design the system such that the resistor network Does not pull down the current source (the source impedance must Be high compared to the load).

A/D Conversion via Successive Approximations



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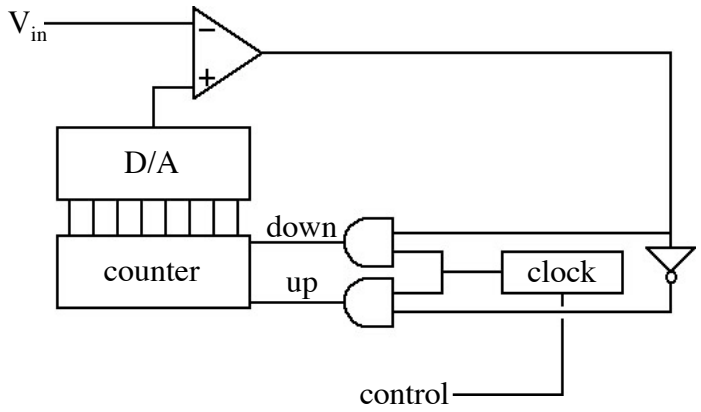
An older approach to A/D conversion is by successive approximations, start with the most significant bit and work your way down to the least. The comparator simply informs if the approximation is too high. You can think about this as a feedback loop looking for its operating point, but in truth it will never be found since the approximation is not equal to Vin.

Tracking A/D Converter

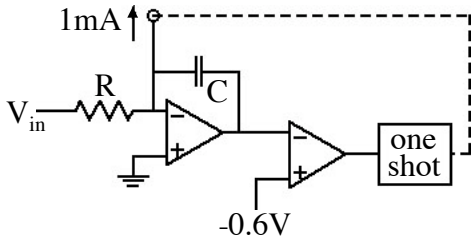


If $V_+ > V_-(V_{in})$, then V_{out} is high and we count down.
If $V_+ < V_-(V_{in})$, then V_{out} is low and we count up.

The closer to V_{in}, the slower the clock; better approximation.

The tracking AD works by the output of a comparator driving the counting direction. The counter outputs a digital word that the D/A converts to V+. The control signal sets the clock rate, so as the counter bounces back and forth around the binary of Vin, the clock is slowed down to get a better representation. The nice feature about the tracking A/D is that is will follow a moving target.

Charge-Balance Converter



- with V_{in} fixed the integration generates a negatively going slope.

$$V_C = \int \frac{V_{in}}{RC}\, dt$$

- V_C equals V_- of the comparator, so when $V_- < -0.6V$, the output of the comparator goes high and triggers the one-shot (monostable).
- The one-shot turns on the current source which draws current off the capacitor. $\Delta q = 1mA \cdot \Delta_{one\text{-}shot}$.
- The entire thing repeats and the system is held in balance if

$$f = \frac{V_{in}}{R \cdot I_S \cdot \Delta_{one\text{-}shot}} \equiv \text{frequency of pulse}$$

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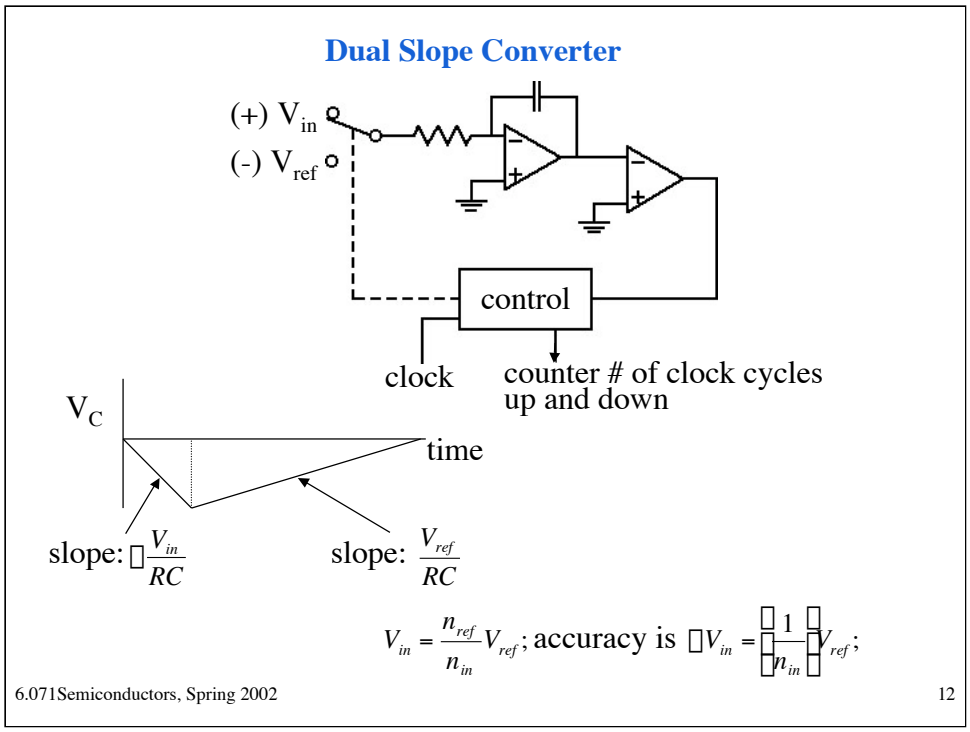
The charge balance design is the most common for low cost, slow devices (but it can be very accurate). The idea is to charge a capacitor via the integrated signal Vin. This is used to trigger a monostable that send a brief trigger pulse to a precise current source. The frequency of the current source will cancel the buildup of charge in the capacitor due to the integrator, and so the frequency provides a measure of the input voltage. The frequency is measured with a counter that is not shown.



The dual slope A/D converter is just a version of the charge balance device, but here a reference counts down and the input up (the switch is of course a FET). By measuring the ratio of the slopes the input voltage can be approximated and the accuracy is related to the number of cycles it counted for the measurement.

Sample and Hold

- Goals: Sample and store a voltage for a time long enough to make repeated measurements (comparisons with).
- During Sampling - Unity gain; high enough slew rate.
- Sample to Hold - There is a transient before a good measurement can be made (5 τ 100ns)
- Hold - avoid droop

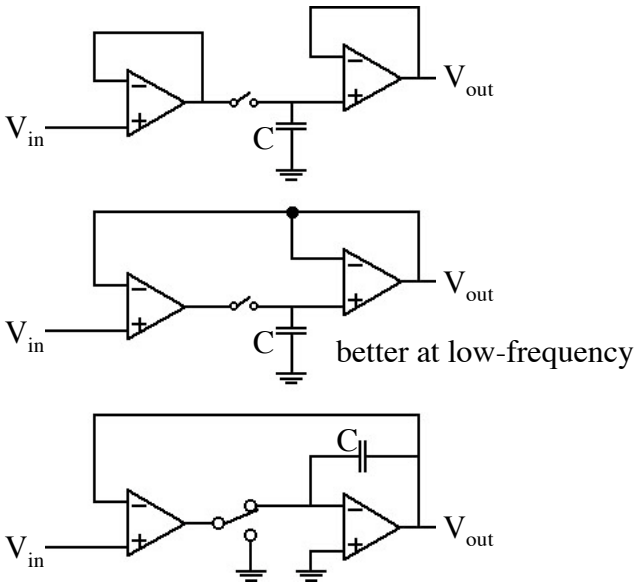
$$\frac{\Delta V}{\Delta t} = \frac{I_{leakage}}{C}$$

C is in pF (fast response) and $I_{leakage}$ in pA (MOSFET technology)

$\frac{\Delta V}{\Delta t}$ is in V/S

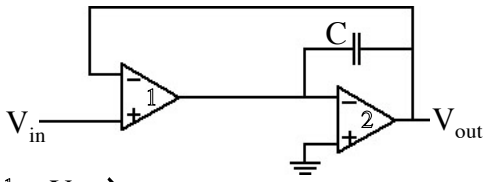
- Feed through - a bit of the input leaks through even though the device is in a hold state.

Sample and Hold Circuits



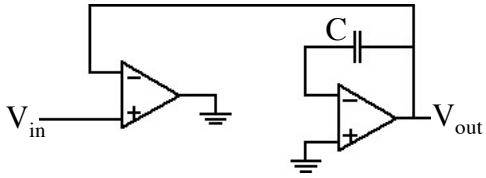
Three versions of a sample and hold. The first two are similar to circuits we've seen before, buffers separating a storage capacitor. The third has the storage cap in the feedback loop.

Sample and Hold Circuits (cont.)



$V_+^1 = V_{in}$
$V_-^1 = V_{out}^2$
$\Rightarrow V_{out}^2 = V_{in}$

$V_+^2 = gnd$
$V_-^2 = V_{out}^1 + V_{out}^2 - V_C$
$\Rightarrow V_{out}^1 + V_{out}^2 - V_C = 0$
$V_{out}^1 = 0$
$\Rightarrow V_{in} = V_C$



A simple analysis of a sample and hold with the storage cap in the feedback loop. Note the output must go into a high impedance load.

TC7129 datasheet #1

MICROCHIP

TC7129

4-1/2 Digit Analog-To-Digital Converter with On-Chip LCD Drivers

FEATURES

- **Count Resolution ..... ±19,999**
- **Resolution on 200 mV Scale 10µV**
- **True Differential Input and Reference**
- **Low Power Consumption ..... 500µA at 9V**
- **Direct LCD Driver for 4-1/2 Digits, Decimal Points, Low-Battery Indicator, and Continuity Indicator**
- **Overrange and Underrange Outputs**
- **Range Select Input 10:1**
- **High Common-Mode Rejection Ratio 110dB**
- **External Phase Compensation Not Required**

ORDERING INFORMATION

Part No.	Pin Layout	Package	Temperature Range
TC7129CKW	Formed	44-Pin PQFP	0°C to +70°C
TC7129CLW	—	44-Pin PLCC	0°C to +70°C
TC7129CPL	Normal	40-Pin PDIP	0°C to +70°C

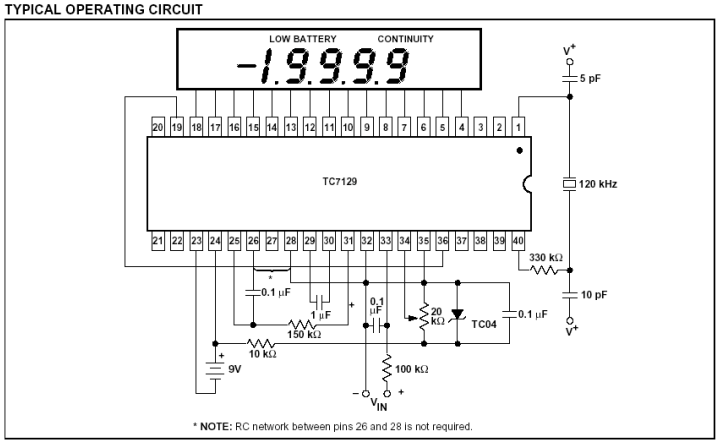
GENERAL DESCRIPTION

The TC7129 is a 4-1/2 digit analog-to-digital converter (ADC) that directly drives a multiplexed liquid crystal display (LCD). Fabricated in high-performance, low-power CMOS, the TC7129 ADC is designed specifically for high-resolution, battery-powered digital multimeter applications. The traditional dual-slope method of A/D conversion has been enhanced with a successive integration technique to produce readings accurate to better than 0.005% of full scale, and resolution down to 10µV per count.

The TC7129 includes features important to multimeter applications. It detects and indicates low-battery condition. A continuity output drives an annunciator on the display, and can be used with an external driver to sound an audible alarm. Overrange and underrange outputs and a range-change input provide the ability to create auto-ranging instruments. For snapshot readings, the TC7129 includes a latch-and-hold input to freeze the present reading. This combination of features makes the TC7129 the ideal choice for full-featured multimeter and digital measurement applications.

TC7129 datasheet #2

TYPICAL OPERATING CIRCUIT



TC7129-5 10/18/96

TC7129 datasheet #3

4-1/2 Digit Analgo-To-Digital Converterwith On-Chip LCD Drivers

TC7129

ABSOLUTE MAXIMUM RATINGS*

Supply Voltage (V^+ to V^-) 15V
Reference Voltage (REF HI or REF LO) ..... V^+ to V^-
Input Voltage (IN HI or IN LO) (Note 1) ..... V^+ to V^-
V_{DISP} ..... V^+ to (DGND – 0.3V)
Digital Input, Pins
1, 2, 19, 20, 21, 22, 27, 37, 39, 40 ..... DGND to V^+
Analog Input, Pins 25, 29, 30 ..... V^+ to V^-
Package Power Dissipation ($T_A \leq 70°C$)
Plastic DIP 1.23W
PLCC 1.23W
Plastic QFP 1.00W
Operating Temperature Range ..... 0°C to +70°C
Storage Temperature Range ..... – 65°C to +150°C
Lead Temperature (Soldering, 10 sec) ..... +300°C

Notes: Input voltages may exceed supply voltages, provided input current is limited to ±400 µA. Currents above this value may result in invalid display readings but will not destroy the device if limited to ±1 mA. Dissipation ratings assume device is mounted with all leads soldered to printed circuit board.

*Static-sensitive device. Unused devices must be stored in conductive material. Protect devices from static discharge and static fields. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to Absolute Maximum Rating Conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS: V^+ to V^- = 9V, V_{REF} = 1V, T_A = +25°C, f_{CLK} = 120 kHz, unless otherwise indicated. Pin numbers refer to 40-pin DIP.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Input						
	Zero Input Reading	V_{IN} = 0V, 200mV Scale	–0000	0000	+0000	Counts
	Zero Reading Drift	V_{IN} = 0V, 0°C < T_A < +70°C	—	±0.5	—	µV/°C
	Ratiometric Reading	V_{IN} = V_{REF} = 1000mV, Range = 2V	9997	9999	10000	Counts
	Range Change Accuracy	V_{IN} = 0.1V on Low Range +V_{IN} = 1V on High Range	0.9999	1.0000	1.0001	Ratio
RE	Roll-Over Error	– V_{IN} = +V_{IN} = 199mV	—	1	2	Counts
NL	Linearity Error	200 mV Scale	—	1	—	Counts
CMRR	Common-Mode Rejection Ratio	V_{CM} = 1V, V_{IN} = 0V, 200mV Scale	—	110	—	dB
CMVR	Common-Mode Voltage Range	V_{IN} = 0V 200 mV Scale	— —	(V^-) +1.5 (V^+) –1	— —	V V
e_N	Noise (Peak-to-Peak Value Not Exceeded 95% of Time)	V_{IN} = 0V 200mV Scale	—	14	—	μV_{P-P}
I_{IN}	Input Leakage Current	V_{IN} = 0V, Pins 32, 33	—	1	10	pA
	Scale Factor Temperature Coefficient	V_{IN} = 199mV, 0°C < T_A < +70°C External V_{REF} = 0ppm/°C	—	2	7	ppm/°C

TC7129 datasheet #4

Power						
V_{COM}	Common Voltage	V+ to Pin 28	2.8	3.2	3.5	V
	Common Sink Current	ΔCommon = +0.1V	—	0.6	—	mA
	Common Source Current	ΔCommon = –0.1V	—	10	—	µA
DGND	Digital Ground Voltage	V+ to Pin 36, V+ to V– = 9V	4.5	5.3	5.8	V
	Sink Current	ΔDGND = +0.5V	—	1.2	—	mA
	Supply Voltage Range	V+ to V–	6	9	12	V
I_S	Supply Current Excluding Common Current	V+ to V– = 9V	—	0.8	1.3	mA
f_{CLK}	Clock Frequency		—	120	360	kHz
	V_{DISP} Resistance	V_{DISP} to V+	—	50	—	kΩ
	Low-Battery Flag Activation Voltage	V+ to V–	6.3	7.2	7.7	V
Digital						
	Continuity Comparator	V_{OUT} Pin 27 = High	100	200	—	mV
	Threshold Voltages	V_{OUT} Pin 27 = Low	—	200	400	mV
	Pull-Down Current	Pins 37, 38, 39	—	2	10	µA

4-1/2 Digit Analgo-To-Digital Converterwith On-Chip LCD Drivers

TC7129

ABSOLUTE MAXIMUM RATINGS*

Supply Voltage (V+ to V–) 15V
Reference Voltage (REF HI or REF LO) ..... V+ to V–
Input Voltage (IN HI or IN LO) (Note 1) ..... V+ to V–
V_{DISP} ..... V+ to (DGND – 0.3V)
Digital Input, Pins
1, 2, 19, 20, 21, 22, 27, 37, 39, 40 ..... DGND to V+
Analog Input, Pins 25, 29, 30 ..... V+ to V–
Package Power Dissipation ($T_A \leq 70°C$)
Plastic DIP 1.23W
PLCC 1.23W
Plastic QFP 1.00W
Operating Temperature Range ..... 0°C to +70°C
Storage Temperature Range ..... – 65°C to +150°C
Lead Temperature (Soldering, 10 sec) ..... +300°C

Notes: Input voltages may exceed supply voltages, provided input current is limited to ±400 µA. Currents above this value may result in invalid display readings but will not destroy the device if limited to ±1 mA.
Dissipation ratings assume device is mounted with all leads soldered to printed circuit board.

*Static-sensitive device. Unused devices must be stored in conductive material. Protect devices from static discharge and static fields. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to Absolute Maximum Rating Conditions for extended periods may affect device reliability.

TC7129 datasheet #5

ELECTRICAL CHARACTERISTICS: V^+ to V^- = 9V, V_{REF} = 1V, T_A = +25°C, f_{CLK} = 120 kHz, unless otherwise indicated. Pin numbers refer to 40-pin DIP.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Input						
	Zero Input Reading	V_{IN} = 0V, 200mV Scale	–0000	0000	+0000	Counts
	Zero Reading Drift	V_{IN} = 0V, 0°C < T_A < +70°C	—	±0.5	—	µV/°C
	Ratiometric Reading	V_{IN} = V_{REF} = 1000mV, Range = 2V	9997	9999	10000	Counts
	Range Change Accuracy	V_{IN} = 0.1V on Low Range ÷ V_{IN} = 1V on High Range	0.9999	1.0000	1.0001	Ratio
RE	Roll-Over Error	– V_{IN} = +V_{IN} = 199mV	—	1	2	Counts
NL	Linearity Error	200 mV Scale	—	1	—	Counts
CMRR	Common-Mode Rejection Ratio	V_{CM} = 1V, V_{IN} = 0V, 200mV Scale	—	110	—	dB
CMVR	Common-Mode Voltage Range	V_{IN} = 0V 200 mV Scale	— —	(V^-) +1.5 (V^+) –1	— —	V V
e_N	Noise (Peak-to-Peak Value Not Exceeded 95% of Time)	V_{IN} = 0V 200mV Scale	—	14	—	μV_{P-P}
I_{IN}	Input Leakage Current	V_{IN} = 0V, Pins 32, 33	—	1	10	pA
	Scale Factor Temperature Coefficient	V_{IN} = 199mV, 0°C < T_A < +70°C External V_{REF} = 0ppm/°C	—	2	7	ppm/°C
Power						
V_{COM}	Common Voltage	V^+ to Pin 28	2.8	3.2	3.5	V
	Common Sink Current Common Source Current	ΔCommon = +0.1V ΔCommon = –0.1V	— —	0.6 10	— —	mA µA
DGND	Digital Ground Voltage	V^+ to Pin 36, V^+ to V^- = 9V	4.5	5.3	5.8	V
	Sink Current	ΔDGND = +0.5V	—	1.2	—	mA
	Supply Voltage Range	V^+ to V^-	6	9	12	V
I_S	Supply Current Excluding Common Current	V^+ to V^- = 9V	—	0.8	1.3	mA
f_{CLK}	Clock Frequency		—	120	360	kHz
	V_{DISP} Resistance	V_{DISP} to V^+	—	50	—	kΩ
	Low-Battery Flag Activation Voltage	V^+ to V^-	6.3	7.2	7.7	V
Digital						
	Continuity Comparator Threshold Voltages	V_{OUT} Pin 27 = High V_{OUT} Pin 27 = Low	100 —	200 200	— 400	mV mV
	Pull-Down Current	Pins 37, 38, 39	—	2	10	µA